A5

Column 2, rewrite line 4 as follows: --transistor, a ~~dielectric~~ resonator, [and] two variable [resistors] capacitors and a ~~variable~~ capacitor diode--.

Column 2, beginning at line 23, please amend the specification as follows:--

Jns B2

A6 Cont.

Referring to Fig. 1 the automatic audio level regulator, referenced by 101, is comprised of an audio level regulating integrated circuit [IC3] ICO. When the output signal of the mainframe of the audio equipment is received, it is transmitted to the input terminal of the [electrical] automatic audio level [regulator IC3] regulating circuit 101, which regulates the [electrical] audio level of the signal to a standard level and then sends the regulated signal to a posterior signal processing circuit. As the signal processing circuit is not within the scope of the present invention, it is not described in detail. The power control circuit, referenced by 102, is comprised of a signal amplifier, a comparator and a transistor. When the comparator of the power control circuit 102 receives a signal, the comparator of the power control circuit 102 immediately turns on the transistor, permitting an external power supply to be connected to the transmitter unit to provide it with the necessary working voltage. When the comparator of the power control circuit 102 receives no signal it immediately turns off the transistor. In this way the comparator is used to differentiate voltage, which comes from the audio signal and either turn on or shut off the system. A power recharge circuit, referenced by 106, is coupled to the automatic power control circuit 102. As long as the automatic power control circuit 102 permits the external power force to run the transmitter, the power recharge circuit 106 is able to charge rechargeable batteries. The external and internal dual [oscillation] adjustable oscillatory frequency regulating circuit, referenced by 103, is comprised of an oscillating transistor OSC, a dielectric resonator DR, and two variable [resistors] capacitors VCA, VCB. As the signal processing

circuit 105 processes the stabilized audio signal, the signal is further sent to IC2 to produce a stereo sound signal which is then is carried by a 19KHz pilot signal to the external and internal dual adjustable oscillatory frequency regulating circuit, reference 103.

The external and internal dual adjustable oscillatory frequency regulating circuit 103 is comprised of a dielectric resonator DR, and two variable capacitors VCA and VCB, as noted above, and a variable capacitor diode VD1.

The input terminal of the external and internal dual adjustable oscillatory frequency regulating circuit 103 is connected to the output terminal of the aforesaid signal processing circuit 105 and the output terminal thereof is connected to the inductance antenna 104. [The input terminal of the oscillation frequency regulating circuit 103 is connected to the output terminal of the aforesaid signal processing circuit, and the output terminal thereof is connected to the inductance antenna, referenced by 104] The inductance antenna 104 itself is a matching device, and therefore no any external matching device is needed. Fine turning the VR1 changes the voltage of the Variable Capacitor Diode VD1 and results in the change of frequency.

When the external and internal dual adjustable oscillatory frequency regulating circuit 103 produces an ideal frequency, it is transmitted to a remote receiver by the antenna, 105.

Referring to Fig. 2, the receiver unit comprises an [oscillation] external and internal dual adjustable oscillatory frequency regulating circuit 201 [(see the left side of FIG. 2)]. The structure of the [input terminal] external and internal oscillatory frequency regulating circuit is identical to that of the transmitter unit. Typically circuit 201 will produce a first intermediate frequency. When the signal from the receiver unit antenna 200 is amplified by

the RF amplifier it is mixed with a first down converted frequency which is internally pre-adjusted by VCA and VCB which results in a first IF. The first IF is provided to the signal processing circuit 202 for a second frequency mixing. The FM OSC further produces an oscillatory frequency to mix with the first IF to produce a resulting second IF.

The input terminal of the internal and external dual adjustable oscillatory frequency regulating circuit 201 is connected to the receiving antenna 200, and the output terminal thereof is connected to the signal processing circuit 202 of the receiver unit. The signal processing circuit of the receiver unit 202 is comprised of an integrated circuit IC-1. The 24-time frequency divider circuit referenced by 204 is comprised of a resistor R-14, and capacitors C25, C26, C27, C28, and C29, and an oscillator[,] . The oscillator is connected to the signal processing circuit IC-1 to divide the frequency of the output signal of the signal processing circuit 24, so as to provide a 19 KHz three-dimensional demodulated signal of better left, right sound track discrimination. When the output signal of the signal processing circuit is amplified it is provided to the speaker [of earphone].

The-.

Rewrite Column 3, beginning at line 1, as follows:

auto-shut off circuit 203 is comprised of an integrated circuit IC-2 and a transistor Q5. The transistor Q5 is controlled by the integrated circuit IC-2 to [turned off] turn the external power supply or battery power supply on and off. The integrated circuit IC-2 can automatically cut off the power supply after a predetermined length of time so as to achieve an energy saving. The working voltage of the receiver unit is designed at a low level of about 2.1-3.5V so that battery power consumption can be minimized.